Evaluation of Chip-to-Board Interconnection Using Variable Aspect Ratio Contact Pad Areas

Pio Jesudoss, Alan Mathewson, William Wright, and Frank Stam

Abstract - This paper describes the evaluation of chip-to-board interconnection for low I/O sensor attachment. In particular the interconnections of different chip and printed circuit board (PCB) pad size ratios with offsets were investigated. Initial assemblies were made using lead-free, 99.3Sn0.7Cu solder. Solder joint shape prediction software, "surface evolver", has been used to simulate the solder joint shape formation for different ratio chip-to-board bond pad areas with different offsets between the two surfaces during the interconnection. The preliminary results show that depending on the solder volume and the aspect ratio of the chip-to-board pads, a convex or concave curvature of the solder joint is observed. Further simulation suggests the pad size plays a major role in the shape of the considered joints.

I. INTRODUCTION

The demand for bare die packaging to have high reliability at reduced cost favours the flip chip (FC) technology over the more conventional wire bonding technology [1], [2]. The flip chip approach was developed by IBM under the name of C4 (controlled chip collapse interconnection) and it has been used in the last number of decades for systems level assembly of integrated circuits onto interconnect PCBs.

FC interconnection occurs when a die is flipped over and the chip bond pads are directly attached to the PCB bond pads via solder or other adhesive interconnection materials. FCOH (Flip Chip Over Hole) is a variant type of FC interconnection, which is mostly used in low I/O count technology such as sensor attachment [2]-[4]. An opening is machined in the PCB to permit interaction between the sensor and the environment it is expected to monitor.

The low I/O bond pad density on the chip can provide an opportunity to use larger bond pad sizes which could be matched up with larger PCB pad sizes. This is interesting because using larger board pad geometries could reduce the direct cost of the board.

In typical IC and system assembly applications, a similar chip-to-board bond pad aspect ratio can be used to achieve a reliable interconnection [5]. Use of Surface Evolver [6] in modelling a Tape Ball Grid Array (TBGA) with a substrate-to-chip pad ratio of 1.18 [7] has been reported. Yeung et al [8] used the Surface Evolver to predict solder joint shape and also showed that a 50% increase in pad size resulted in the reduction of the standoff height for parallel chip-to-boar pads. However, no studies have been reported on the impact of using variable chip-to-board pad ratios with offsets resulting in non-symmetrical joint shapes. The work presented here aims to study the shape of the solder joints of variable aspect ratio pads through comparison of a model developed within the Surface Evolver of variable chip-to-board pad ratios in a bare die. The study is interesting because it provides information on the effect of volume and the effect of variable chip-to-pad ratio on the shape of the joint. In the next section, a detailed review of the chip, substrate and the FCOH packaging will be presented. This is followed by results, a discussion and conclusions.

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II. EXPERIMENTAL METHODOLOGY

A. The Silicon Test Vehicle

The chip developed in this research has an I/O count of 5, which are located on the periphery of a 6x6mm die as shown in figure 1.a, with the overall FCOH technology shown schematically in figure 1.b. Instances of three different square chip bond pad sizes have been fabricated and these have been used in this work. The pad sizes were 100µm, 300µm, and 500µm. In the chip fabrication, the costly UBM (Under Bump Metallisation) step was eliminated by using a gold finish, as shown in figure.1.c. The second and the third picture in figure 1.c are simple representations of the variable interconnection areas that are involved in this study.

B. Substrate

A thin 0.25mm FR4 board was fabricated with a pad metallization scheme comprising 64.8µm Cu, 5µm Ni and 0.2µm of electroplated flash gold, as shown in figure 1c. A square window of 4.4mm was cut in the centre of the board to enable the chip to be exposed to the surrounding environment after assembly.

C. Assembly

A rigorous pre-cleaning procedure was carried out on both the chip and the substrate. This step was carried out to

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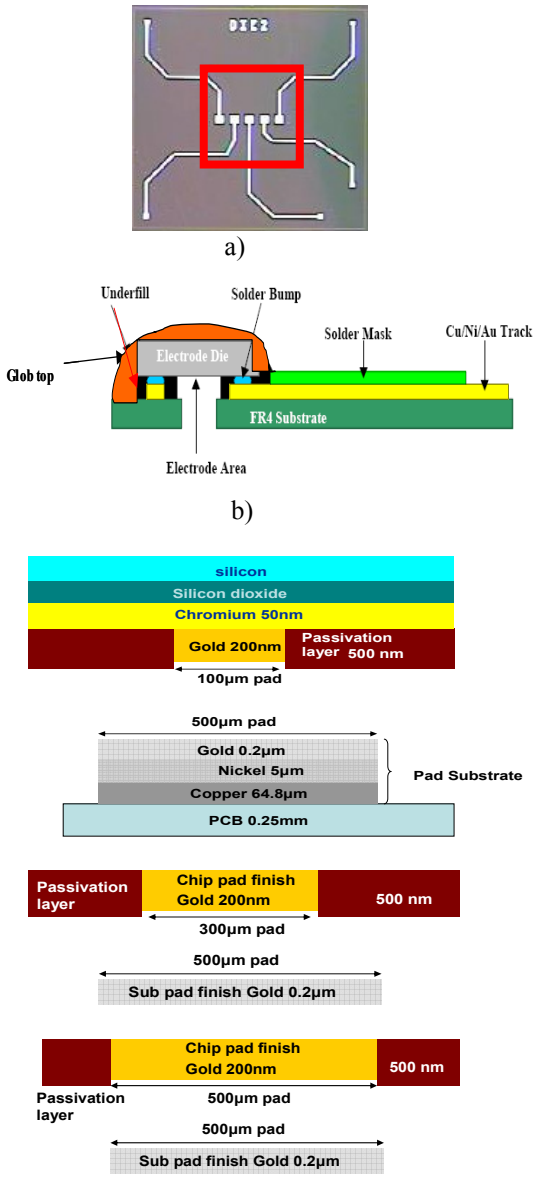


Fig. 1. a) 6x6mm test chip used in the Flip Chip Over Hole (FCOH) development without passivation layer (board opening area indicated); b) Schematic of FCOH technology; c) Schematic of different chip-board contact pad ratio with the chip finish (top to bottom: ratio $chip_{pad}/sub_{pad}$ 0.2, ratio $chip_{pad}/sub_{pad}$ 0.6 and ratio $chip_{pad}/sub_{pad}$ 1.

eliminate any traces of grease, dirt and other contamination that could have occurred during manufacturing process. The pre-cleaning procedure involved placing the chips and the substrates in oxygen plasma for 40sec. This was followed by placing them in IPA in an ultrasonic bath for 5 min followed by a DI water rinse. Then the samples were dried in an oven at 150˚C for an hour. A post cleaningprocedure was carried out to eliminate flux residues and other contaminations. The post-cleaning procedure involved placing the chips and the substrates in chloroform in an ultrasonic bath for 5 min followed by a DI water rinse. This was followed by placing it for 5 min in IPA in an ultrasonic bath. Finally a DI water rinse was carried out and the samples were dried in an oven at 150˚C for an hour. In this post clean chlorinated solvents are used to eliminate the flux [9] residues while IPA and DI water are used to eliminate the ions and other contamination.

63Sn37Pb and 99.3Sn0.7Cu solder paste were dispensed on to the substrate bond pad using CAM/ALOT 1414 liquid dispense system.

A high accuracy Finetech (Finetech Fineplace 96 Lambda) flip chip bonder was used to align and bond the chip to the board bond pads. Figure 2 presents the temperature profile used for 99.3Sn0.7Cu .

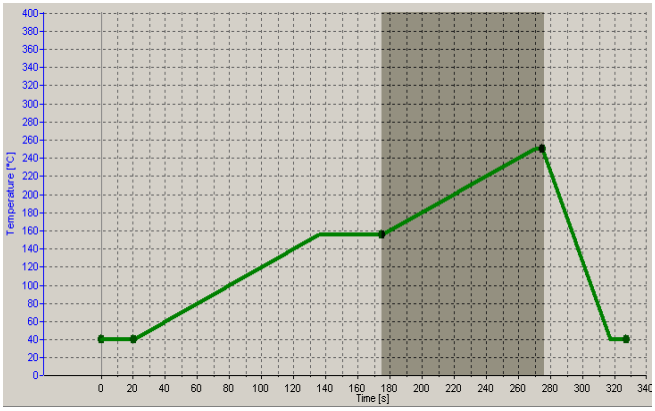


Fig. 2. Temperature profile used for 99.3Sn0.7Cu

To protect the solder interconnection from the liquid measurement environment and to provide mechanical strength, an underfill (Loctite - Hysol FP453) was used. Underfill was dispensed using the earlier mentioned CAM/ALOT dispense system after heating the assembly at 100˚C for 5 min. The curing of the underfill was carried out in a nitrogen purged oven at 150˚C for 90 minutes.

D. Simulation – Surface evolver based methodology.

The Surface Evolver is an interactive modelling tool [6], which models surfaces shaped by different constraints and energies. An initial surface can be defined in a data file and in the Surface Evolver it becomes possible to visualise the evolution of the surface towards its minimal energy by a gradient descent method. The energy in the Evolver can be a combination of surface tension, gravitational energy, squared mean curvature, user-defined surface integrals, or knot energies.

In the data file, the basic geometric elements used to represent a surface are vertices, edges, facets, and bodies. Vertices are points, edges are straight line segments joining pairs of vertices, and facets are flat triangles bounded by three edges. A surface is a union of facets and a body is defined by its bounding facets. The term “surface” refers to all of the geometric elements plus supplementary data such as constraints, boundaries, and forces. A surface has a total energy which arises from surface tension, gravitational energy, and possibly other sources. It is this energy which the Evolver minimizes.

In the case of modelling liquid solder, the energies that are taken into account are the surface tension, the gravitational energy and the external energy due to the applied loads such as the weight of the package [10]. As opposed to most Ball Grid Array (BGA) packages the bare die is considered in this technology and therefore the external pressure from the weight of the chip could be excluded from equation 1 given below.

$$E = \int_V \rho g z dV + \int_S T dS \qquad (1)$$

where ρ, g are the corresponding solder density, gravity and z the height between the $chip_{pad}$ and $substrate_{pad}$. V represents the volume of solder, T the surface tension and S the solder surface. E is the total energy corresponding to the standoff height.

III. Results and Discussion

A. Comparison of solder shape geometry and simulation

Figure 3 shows the cross section of a chip-to-board interconnection with variable aspect ratio contact pad areas and the corresponding geometrical simulation images. In figure 3.a 100 µm $chip_{pad}$ is interconnected to a 500 µm sub_{pad} , thus a small aspect ratio of 0.2 is achieved. The simulated solder shape formation correlates well with the observed shape from the cross section (taking into account the offset between the two surfaces used during the interconnection as shown in figure 4).

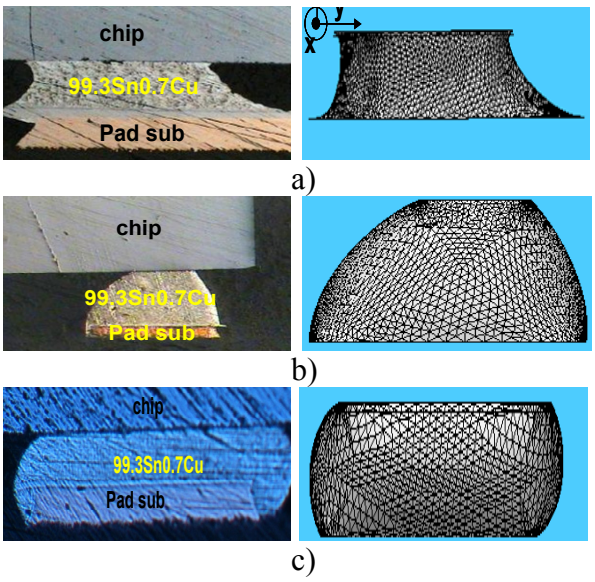
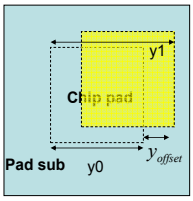


Fig. 3. Cross section and corresponding simulation images of a) ratio $chip_{pad}/sub_{pad}$ 0.2 b) ratio $chip_{pad}/sub_{pad}$ 0.6 c) ratio $chip_{pad}/sub_{pad}$ 1.

The above results indicate that the standoff height varies with the volume of solder dispensed on the board. The results shown in Table I indicate that the convex shape observed for the $chip_{pad}/sub_{pad}$ ratio of 0.2 was due to the large contact area of sub_{pad} available for the solder to spread in comparison to the small contact area of $chip_{pad}$, and hence the curvature of the solder fillet becomes smaller in the cross section (figure 3.a) [8], [11], [12]. The increase in $chip_{pad}$ provides a larger contact area and helps the solder spread to be more or less the same in $chip_{pad}$ and sub_{pad}. The increase in $chip_{pad}$ demands a high solder volume, which in combination with large contact area leads to a convex shape as shown in figures 3.b and 3.c. It also shows the offset used during the interconnection of the chip-to-board pads, the offset being calculated from the position of the chip pad to the substrate pad as shown in figure 4.



$$y_{offset} = y1 - y0$$

Fig. 4. A schematic of the top view of $chip_{pad}$-to sub_{pad} showing the offset and the offset calculation equation.

TABLE I
STANDOFF HEIGHT AND SOLDER VOLUME CORRESPONDING TO THE INTERCONNECTION CHIP-TO-BOARD PAD

Ratio $chip_{pad}/sub_{pad}$	H (mm)	Vol (mm^3)	Offset In y direction
0.2	0.25	0.09	1 –y direction
0.6	0.5	0.3	0.2 +y direction
1	0.4	0.32	0.04 +y direction

B. Prediction of optimum joint shape for each chip-to-board aspect ratio

A theoretical calculation was carried out to obtain a similar standoff height for all of the aspect ratio chip-to-board pads in this study. Table II shows the optimum volume to be dispensed in order to get a similar standoff height while matching different chip-to-board bond pads with similar offsets mentioned in Table I. Figure 5 shows the profile to be expected when using the ideal solder volume as a function of chip and board pad sizes.

TABLE II
OPTIMUM VOLUME CORRESPONDING TO THE INTERCONNECTION CHIP-TO-BOARD PAD

Ratio $chip_{pad}/sub_{pad}$	H (mm)	Vol (mm^3)	Offset In y direction
0.2	0.15	0.0024	1 –y direction
0.6	0.15	0.0071	0.2 +y direction
1	0.15	0.016	0.04+y direction

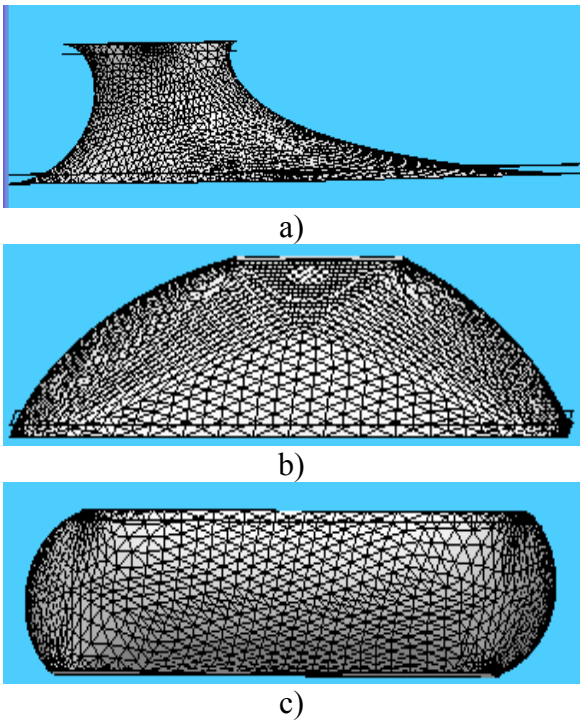


Fig. 5. Simulated results for optimum solder volume a) ratio $chip_{pad}/sub_{pad}$ 0.2 b) ratio $chip_{pad}/sub_{pad}$ 0.6 c) ratio $chip_{pad}/sub_{pad}$ 1

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The preliminary results from Table II and the simulations shown in figure 5 indicate that with the chosen offset, a similar convex and concave solder shaped joint can be expected. With optimum volume for a fixed standoff height, the pad size plays an important role in shaping the solder joint during reflow.

III. Conclusion

This work involved the evaluation of chip-to-board interconnection for low I/O counts. Solder joint shape prediction model "Surface Evolver" has been used to verify the obtained shape during the interconnection of variable chip-to-board pad ratio with offset resulting in non-symmetrical joint shapes. There is a good correlation between the predicted shape and the observed joint shape.

Further simulation suggested that the parameter playing a significant role in the shape and curvature of the shape of the joint is the actual pad size.

Ongoing work is involved in obtaining an optimum solder shape with variable chip-to-board pad ratio with the given offset as a good solder joint is essential for providing a robust a reliable contact. Future work would incorporate the optimum shape solder joints in ANSYS to study the reliability of the joints as a function of thermal and mechanical stresses.

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