

# Can charge writing aid nanotechnological manipulation?

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**Abstract.** Significant progress in the examination or manipulation of submicrometre particles and large molecules is likely to be dependent upon a suitable method in locating and orienting them onto working substrates. Ideally this would be a general purpose tool that allowed local programming to attract selectively species of interest. Charge writing onto electrets with a scanning-probe microscope offers one possible method. Here the use of this technique for memory applications (the only significant body of research) is examined in order to judge the feasibility of using it with different operational parameters for 'electrostatic clamping'. Until recently it was not regarded as practicable, but new materials developments, especially oxide-nitride-oxide-silicon electrets, show considerably more promise. A clear answer to our question cannot yet be given, but further investigations are suggested and recommended.

## 1. Introduction

The manipulation and identification, for size and shape as well as composition, of submicrometre particles and large molecules is of increasing scientific and commercial interest, as there are many possible applications across a wide range of disciplines. Examples include tribology, medical diagnosis, chemical recognition, the promotion of specific reactions and 'molecular assembly' of nanoscale structures. There appear to be fewer successful biological applications of scanning-probe microscopy than we might expect from such a versatile technology, perhaps because it is difficult to hold organic molecules onto a flat substrate [1]. Although their mobility can help in identification, a means of temporary fixing, ideally with some specificity, would be very useful. Similarly, if molecular assembly is to become widespread in the future, the nanotechnological equivalent of a clamp or vice will be needed: self-assembly through the techniques of chemistry in solution is probably the only practical large-scale approach, but it is unlikely to provide solutions for all the challenges of research and development programmes. A convenient, programmable method of gently fixing (in location and orientation) small structures onto substrate surfaces would be of enormous interest. As many chemical and biological processes are mediated by electrostatic forces at 'docking sites' for one molecule on another, we now ask whether a simulation of this process could be used for manipulation. The idea of 'writing' a charge pattern onto a substrate is an obvious approach.

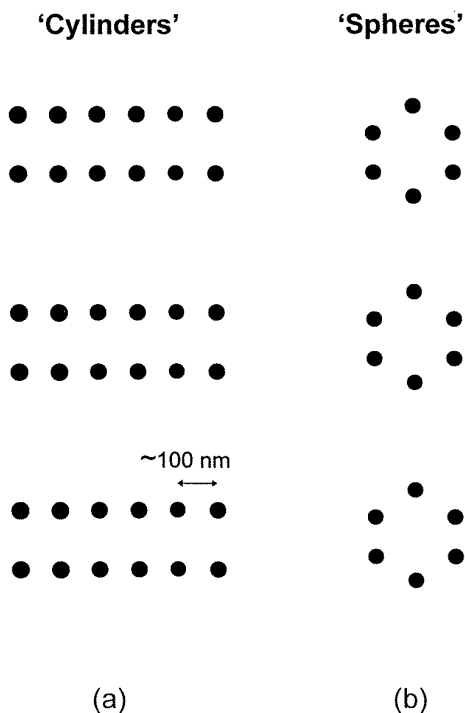
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There is a considerable body of published work concerning charge writing (and re-reading) onto surfaces, especially using forms of scanning-tunnelling microscope (STM) or atomic-force microscope (AFM) but it concentrates almost exclusively on applications to data storage. The operational requirements for 'nanoclamping' are quite different to those for bulk memory applications, and so our purpose here is to look for approaches worth further study by means of a selective review. We emphasize that this paper is not attempting to review charge writing research as such, but instead examines work that appears most relevant to holding and manipulating nanoscale objects. A brief historical review of some material is included because it helps to show why surprisingly little attention has been paid to non-memory applications.

## 2. Requirements for nanomanipulation

Chemical methods are effective for fixing many molecules and nanostructures for analysis but they are less satisfactory for manipulation. Preparation times of substrates can be lengthy and release can be destructive. Electrostatic docking sites at the molecular level could allow non-destructive release after initial binding, since that is what happens in many natural biological processes, and so simulating this approach looks attractive. It would be extremely challenging to current technology to provide patterns reliably on such a small scale, but there is much potential for suitably shaped electrostatic charge fields of 10 to 100 nm resolution and extending over regions of up to several micrometres. Specificity in the sense of chemical docking sites would be ideal, but much weaker conditions

### Charge Patterns for Selecting & Aligning



**Figure 1.** Patterns of charge for locating (and orienting) cylindrical or spherical particles.

by which particles are encouraged to sit in regular arrays or in predefined orientations are also valuable. The concept is illustrated in figure 1, which shows how local charges might be deposited to differentiate between cylindrical and spherical particles. Not all micromechanical methods of data storage involve the direct use of localized charge and only those that do could be of potential use for manipulation. When charge is used there are several ways of injecting it. Thus we should first consider in what ways the needs of data storage and nanoclamping differ and whether this restricts the choice of technologies.

It is essential that the charge field projects above the substrate surface at a useful intensity, whereas some memory methods detect charge effects buried quite deeply. It is also important for biochemical applications that patterns survive for a useful time with substrates immersed in aqueous solutions. If the long-term concern is with a general purpose method applicable to many practical situations it is strongly preferable to have standard substrates onto which user-specified charge patterns can be written as needed. It is also preferable that patterns be erasable. Provided writing is to be performed locally (at reasonable cost), there may not be a need for long charge lifetimes, with even a few minutes being useful and a few hours sufficient for most applications that can be envisaged. High writing speeds are much less important than for memories both because the amount of data ('bits' of charge) will generally be quite low and because the total writing time can be comparable to the time taken in mounting and then removing the substrate from the writer. There may be applications where mass-produced standard patterns

are wanted and then writing speeds and storage lifetimes should be closer to those needed for memories. Finally we note that memories are digital systems, which can tolerate considerable signal degradation, whereas location and manipulation make explicit use of the field shape and so depend much more directly on the level of charge stored at each point. Care must be taken in interpreting the results of digital experiments for use in applications where analogue levels are significant.

To contemplate local pattern writing at reasonable cost, the equipment needed must be relatively compact, easy to use and have low service overheads. Only methods based on scanning probe microscopes (SPMs) offer serious hopes of meeting these criteria and it is upon those that this work concentrates. We assume there to be no need to review the working of these instruments as they are now well established laboratory tools. Very briefly, they derive from pioneering work by Young and colleagues who, starting from a non-contact distance and displacement measuring instrument, based on the field emission of electrons between tip and sample in close proximity when a bias voltage exists between them, proposed a new device for measuring surface microtopography (the 'topografiner') [2]. This idea was too demanding of the technology then available. It was some years before the now familiar form of the STM, in which topography is determined from the signal needed to keep the probe at a constant height (constant tunnelling current) while being scanned over a surface, produced the first results with atomic resolution, showing the  $7 \times 7$  reconstruction of the surface of Si(111), which had been predicted in theory but had not been demonstrated experimentally [3]. The STM concept has changed little since then, although operational convenience has been improved and the cost greatly reduced: the most significant advance was the use of a piezoelectric tube-scanner [4] to move the tip, rather than separate piezoelectric elements for each axis.

In 1986, after receiving the Nobel Prize for the STM, Binnig developed the AFM [5], consisting of a flexible cantilever or stylus which could be scanned over the sample. Forces acting between the tip and surface cause the cantilever to deflect—the great advantage of this technique over the earlier STM was that non-conductive materials could be investigated. The motion of the stylus was originally measured using an STM tip above the cantilever, although AFMs now measure this deflection using photodiodes, capacitance sensing, optical interferometry or cantilevers made from piezoresistive or piezoelectric materials. The basic AFM may be used in contact mode, where the interatomic forces are repulsive in nature, in non-contact mode, where the tip-sample spacing is larger and the interatomic forces are attractive in nature, or in intermittent contact mode, which combines these two [6].

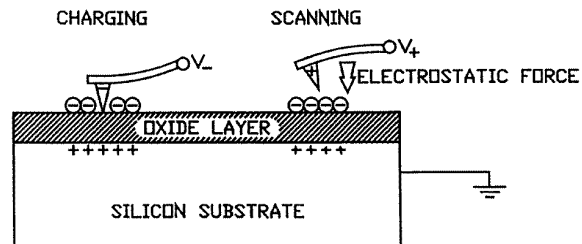
The AFM and STM have spawned many other probe microscopies [6], and there are several comprehensive reviews in the literature of STM techniques [7] and other probe devices such as AFMs and near-field scanning optical microscopes (NSOMs) [8]. Two techniques that are used to measure stored electric charges or dielectric constants

are of particular relevance to this study. Electrostatic force microscopy (EFM) uses a bias voltage applied between a conducting cantilever tip and the sample, without the tip touching the surface. The cantilever then deflects when it is scanned over static charges, which attract or repel the tip. The magnitude of the deflection is proportional to the charge density, and both positive and negative charges may be differentiated. The standard photodetector system of an AFM may be used. Structurally similar to the EFM, in scanning capacitance microscopy (SCM) the cantilever operates in constant height, non-contact mode with a bias supplied between tip and sample. The capacitance between tip and sample is monitored, and this is dependent on the dielectric properties of the medium between them.

SPM technology has not been restricted to measurement applications: STMs or AFMs have long been used as micromechanical tools on a submicrometre or nanometre scale. Typically surface modification and atomic transfer was achieved by applying voltage pulses (larger than the normal bias) to a tip [9]. Early work looked at nanolithographic applications, for example in layers of calcium/aluminium fluoride deposited on a substrate of silicon [10]. A similar method was used to modify the surface of germanium on an atomic scale, under ultra-high vacuum (UHV) conditions [11]. The STM has also been used to pin individual molecules onto a highly orientated pyrolytic graphite (HOPG) substrate by applying a bias voltage through a thin layer of liquid polymer [12]. Possibly the first (and most highly publicized) application of atomic manipulation enabled the precise positioning of individual xenon atoms on a (110) nickel surface to create the letters 'IBM', again in UHV and cooled to 4 K [13]. This process was also applied to semiconductors, and individual silicon atoms could be removed from and deposited on a Si(111)-7x7 surface [14], and individual dimers moved or 3 nm wide trenches created on Si(100) surfaces [15]. A variety of recent developments in technique may be found in [16]. Very recently an AFM has been used directly to provide small features using a polishing-like process [17]. None of this work directly addresses our topic since it does not involve local charge storage. However, it demonstrates a potential to provide locally modified topographies on which charge might be written to give a more subtle control of the field. Practical exploitation of this idea first requires the realization of a useful method of using charge storage for basic manipulation.

### 3. SPMs for memory (charge storage) applications

The capability of SPMs to modify or manipulate matter on the nanometre or even atomic scale has long fuelled interest in the use of an SPM for high density data storage applications. Many different techniques have been suggested [18]. Some rely on a physical change in the surface topography, such as the deposition of mounds or dots by STM on a variety of conducting or semiconducting materials, with AgSe [19], Ag(111) [20] and Au(111) [21,22] all showing potential data storage capabilities.



**Figure 2.** Schematic representation of contact electrification.

However, these techniques are non-reversible and would be unable to generate electrostatic location sites since they are charge-neutral. Vanadate glass on a vanadate bronze substrate was shown [23] to produce small erasable features but they were attributed to a localized transition between amorphous and crystalline phases in the material.

There has, however, been a great deal of research investigating techniques which utilize a local change in electrical conductance or physical non-volatile charge storage in an electret structure having a thin insulator layer upon a more conducting substrate [24]. Much of this work has examined the suitability of different substrate materials or electrets, a typical review is given in reference [25]. The materials used may be conveniently grouped into five categories, corresponding to the following sections. The principle data, with specific parameters, dimensions and conditions from each reference, is summarized in the corresponding tables 1–5.

#### 3.1. Polymer films

There has been considerable interest in the use of polymer films to store charge, as they are effective insulators and electret materials. Early work used a scanning force microscope with an etched wire tip to deposit charge in 1 mm thick polymethyl-methacrylate (PMMA) by corona discharge using 100 V pulses [26,27]. The charged areas were 2  $\mu\text{m}$  in diameter, and decayed after approximately 1 hour. Later work by the same authors used contact electrification (see figure 2 and section 3.2) and lower voltages (5 V) to achieve similar results [28]. Other work using PMMA [29] produced much smaller charged areas, 70–300 nm in diameter, using a 50 nm radius tip and a spun polymer layer 300 nm thick. The smallest charge-induced changes to a polymer film reported were 10 nm in diameter [30], but were attributed to conductance changes in the polyimide Langmuir–Blodgett film used, rather than stored charge. A study of the parameters used in contact electrification such as the applied voltage, number of contacts and their duration [31] showed that the amount of stored charge (i.e. the charge density) was proportional to the applied voltage but not to the number of contacts. However, no systematic, quantitative study has been performed regarding the diameter of the charged areas with respect to these parameters.

Some of the more promising work used plasma-polymerized films of acetylene and hydrocarbons 2–10 nm

**Table 1.** Summary of charge storage applications in polymer films.

Reference	Film material	Film thickness	Deposition technique	Substrate	Applied voltage	Pulse duration	Tip	Bit size	Notes
[32]	acetylene/hydrocarbon	2–10 nm	pulsed discharge plasma polymerisation	n-type Si(100) 3–6 Å cm	40 V	20 s	Au coated Si <sub>3</sub> N <sub>4</sub> AFM 50 nm radius	13–25 nm	surface indentation after 15 V no charge deposition below 30 V
[34]	organic 'dots' of TTPAE and Diamine	0.5 nm dot thickness, 20 nm dot radius	vacuum evaporation	p-type Si with 20 nm SiO <sub>2</sub> < 0.01 Å cm	1 V	< 1s	Cr/Au coated Si <sub>3</sub> N <sub>4</sub> AFM 30 nm radius	30 nm FWHM	contact electrification
[30]	polyimide Langmuir-Blodgett	3 nm (6 monolayers 0.5 nm)	thermal imidation of polyamic acid	gold electrode on mica	3.6 V	500 μs	STM	10 nm diameter	attributed to change in conductance of the L-B film
[29]	PMMA	300 nm	spin coated	degenerately doped GaAs	10 V	10 ms	STM/SFM 50 nm radius	70–300 nm diameter	70 nm—corona discharge; 300 nm—contact electrification
[26]	PMMA, sapphire, mica and quartz	PMMA—1 mm	PMMA was solvent-cleaned	none	100 V	25 ms	SFM 5 μm etched Ni wire	2 μm diameter	corona discharge, 1 hour decay, quartz/mica decayed in seconds
[28]	PMMA	1 mm	protective coating removed	none	0 V or ±5 V	4–5 s	SFM 10 μm etched Ni wire	2–10 μm diameter	unbiased contact 10 μm; biased contact 2 μm.
[31]	PMMA	1 mm	—	none	0–15 V	1–5 s	etched W wire	2–10 μm FWHM	study of voltage, no. of contacts and duration, and offsets.
[27]	PMMA	1 mm	—	none	100 V	25 ms	etched 10 μm Ni wire	5–10 μm	similar work to [31] by the same authors
[33]	polyfluorinated cyclo oxaliphatic polymer	2.1 μm	spun	indium-tin oxide on glass	300 V	1 ms	AFM 50 μm etched W wire	FWHM 280 nm	charges decayed over 8 h

**Table 2.** Summary of charge storage applications in silicon oxide structures.

Reference	Silicon substrate	Oxide thickness	Formation method	Voltage	Duration	Tip	Bit size	Duration	Notes
[35]	p-type (111) 0.002–0.005 Ω cm	—	native oxide	scanning 5 V	2–12 h	tungsten STM	—	—	oxide layer removed by high voltage STM scanning
[36]	p-type (100) 10–20 Ω cm; n-type 8–12 Ω cm	3–6 nm	thermally oxidized in dry O <sub>2</sub>	±4 V	—	AFM Cr and Au coated 25 nm radius	≈ 2 μm	7.5 min	experiments observed contact electrified charge decay over time
[37]	p-type (100) 10–20 Ω cm	5.4 nm ±0.1 nm	thermally oxidized in dry O <sub>2</sub>	±4 V, ±8 V and ±10 V	30 s	AFM Cr and Au coated 25 nm radius	≈ 2 μm and FWHM of 600 nm	7.5 min	higher voltages produce time dependent dielectric breakdown of the SiO <sub>2</sub> layer
[38]	p-type (100) 10–20 Ω cm	5.7 nm ±0.4 nm	thermally oxidized in dry O <sub>2</sub> ; heat treated; steamed	±4 V	20 s	AFM Cr and Au coated 25 nm radius	FWHM 188–424 nm	1000 s	FWHM 424 nm before heating; 188 nm after heating; 212 nm after steaming
[40]	p-type (100) 10–20 Ω cm	5.4 nm ±0.1 nm	thermally oxidized in dry O <sub>2</sub>	–2 to –5 V	3–360 s	AFM Cr and Au coated 25 nm radius	≈ 2 μm	7.5 min	determined effects of varying contact time, contact voltage and measurement voltage
[41]	n-type (100) 8–12 Ω cm	7, 20 and 460 nm	thermally grown in dry O <sub>2</sub> (7nm) and humidified N <sub>2</sub> (20 and 460 nm)	—	—	Electron beam lithography 300 keV 1 nm	100–200 nm	months	no charge trapping was observed in the thinner oxides
[39]	p-type (100) 10–20 Ω cm	5.7 nm ±0.4 nm	thermally oxidized in dry O <sub>2</sub>	–4 V	40 and 20 s	AFM Cr and Au coated 25 nm radius	≈ 2 μm	—	measured the effects of proximity between two charged spots up to 2 μm apart

**Table 3.** Summary of charge storage applications in NOS structures.

Reference	Silicon type	Oxide layer forming method	Oxide thickness (nm)	Nitride layer forming method	Nitride thickness (nm)	Pulse amplitude (V)	Pulse duration (μs)	Tip	Bit size/ resolution	Storage duration/ lifetime
[43]	n-type 0.42 Å cm	CVD	5–9	CVD	40–50	±40	0.1	10 μm flat square area	50 μm <sup>2</sup>	> 10 h
[44]	boron-doped p-type Si (100) 0.2, 1.8 and 16 Å cm	HC1 etch	1–2	LPCVD	50	–40 V write/ 10 V erase	100/20	80–100 nm radius	75–150 nm FWHM	1/e in 1 h
		30 min 800 °C dry oxygen	3–5	LPCVD	50	40 V write/ 40 V erase	100/1000	80–100 nm radius	75–150 nm FWHM	> 7 days
[24]	boron-doped p-type Si (100) 1.8 Å cm	30 min 800 °C dry oxygen	3–5	LPDVD	50	–40	20	80–100 nm radius	75–150 nm FWHM	
[46]	p-type Si 1 Å cm	thermally grow	3.9, 4.4 and 6.6	CVD	44.7	–40	90, 70, 50, 30, 10, 1	80–100 nm radius	> 150 nm for 1 μs pulse	> 9 months at 150 °C
[47]	p-doped Si (100) 10–20 m Å cm	grown	5.1, 6.6 and 8.2	deposition	52–53	–35–38	100 to 20	cantilevers cut from 5 μm W foil then etched	variable down to approximately 60 nm	

**Table 4.** Summary of charge storage applications in ONOS structures.

Reference	Substrate	Base oxide	Nitride	Top oxide	Applied voltage	Pulse duration	Tip	Bit size	Notes
[48]	p-type Si (100) 15–16 $\Omega$ cm	4.7 nm	9.2 nm	2–3 nm	–4 V	20 s	Au/Cr coated Si <sub>3</sub> N <sub>4</sub> AFM	500–3000 nm FWHM	contact electrification
[49]	n-type Si	2.1 nm	10 nm	4 nm	–9 V +10 V	2–10 ms	metallized AFM	100 nm diameter	bit size determined by pulse duration and voltage

**Table 5.** Summary of charge storage applications in other relevant materials.

Reference	Material	Thickness	Applied voltage	Pulse duration	Tip	Bit size	Notes
[23]	vanadate bronze and glass	10 nm	4 V	1–10 ms	STM	10 $\times$ 10 nm	phase change in material, not stored charge
[19]	Ag <sub>x</sub> Se	15 nm	1–5 V	continuous d.c., computer generated template	Pt STM	10 nm	chemical etching, not charge storage
[50]	SrTiO <sub>3</sub>	100 nm	$\pm$ 4 V	20 s	Au/Cr coated Si <sub>3</sub> N <sub>4</sub> AFM	FWHM 70 nm	charges decayed after 17 minutes
[51]	p-type WSe <sub>2</sub>	—	2.3–6 V	several ms	STM	< 1–8 nm	are these charges?

thick and contact electrification [32]. Spot sizes of 25 nm were possible, although some indentation of the surface occurred during the charging process with the AFM tip. Another study investigated the use of a spun polyfluorinated polymer film 2.1  $\mu$ m thick [33] which supported charged regions 280 nm FWHM for 8 h, but could be easily erased by a simple contact with an earthed conductor.

Much smaller spot sizes were obtained by using organic dot structures [34]. Molecules of TTPAE and Diamine were vacuum evaporated onto silicon substrates to form organic dots approximately 20 nm in diameter. These could be selectively charged with a conducting AFM cantilever and bias voltages 0.6–2.0 V for 1 s. The stored charges were reported to remain for tens of hours, but no long term study was undertaken. The charged regions varied in diameter between 30–80 nm (FWHM) depending on the contact voltage: high voltages tended to transfer charge to areas outside the organic dot.

### 3.2. Single silicon oxide layer electrets

There has been considerable work on the charge storage properties of a single layer of silicon oxide on a silicon substrate. Charge can be deposited and the surface scanned using an STM, but it has been shown that the oxide layer can be damaged or even removed [35], which makes the use of an STM relatively unsuitable for charge storage.

However, charge writing using AFMs and contact electrification has been quite successful, and its mechanisms

extensively studied [36–39]. The technique uses a conducting AFM cantilever with a d.c. bias voltage to inject electric charges into a substrate without any current flow (as is the case with STM). The cantilever deposits a local region of contact-electrified charge on the surface of the silicon oxide when the two are touched together. The tip of the cantilever is then withdrawn by 50–70 nm and the sample scanned in non-contact d.c. mode by the AFM. The charged regions on the surface cause the biased cantilever to deflect, i.e. operating as an EFM. This is shown schematically in figure 2, where a typical oxide layer thickness would be 3–6 nm.

Initial work looked at charges in oxide layers of different thickness [36], which had decay times of up to 7 min. Others examined the effect of higher voltages and dielectric breakdown [37], contact time, contact voltage and measurement voltage [40], and the proximity effects between two charged regions [39]. The presence of adsorbed water in the oxide layer was also investigated [38], using heat treatment to dry the layer and steam to reintroduce moisture: dry oxide produced smaller, more compact charged regions. Overall, this method of charge storage is not well suited to applications in nanomanipulation—the charges dissipate within minutes, and charged areas in close proximity tend to merge, thus making the deposition of more complex charge patterns unlikely.

Charges have also been injected using a 300 keV electron beam focused to a 1 nm spot [41]. Although only

successful in relatively thick (460 nm) oxide layers, the resolution obtained was of the order of 100–200 nm and the charged patterns remained for months. However, the oxide was either etched or considerably swollen (~10%) during the process and only positive charges could be stored, as the lower energy negative charges were annealed out by the 200 °C substrate temperature required to prevent surface contamination during irradiation. With more development this technique might be useful for laying down the charge patterns in a mass-production application.

### 3.3. NOS (nitride-oxide-silicon) structures

This approach is based on the metal-insulator-semiconductor (MIS) and metal-nitride-oxide-silicon (MNOS) memory field effect transistor (FET). The structure of these devices is shown schematically in figure 3(a), where a layer of silicon oxide 3–10 nm thick on a silicon substrate is covered by a layer of silicon nitride typically 40–50 nm thick. By placing a metal electrode on the nitride surface and applying a transient voltage between the electrode and the silicon substrate, charge carriers can be made to tunnel through the insulating oxide layer and become trapped in the nitride layer. A comprehensive review of articles concerning these devices is given in [42].

The first attempt at a large capacity memory storage device used a rotating NOS disk with a stationary 'metal' electrode of tungsten carbide [43], and 'bit' sizes were of the order of  $10\ \mu\text{m} \times 5\ \mu\text{m}$  due to the large flat tip. However, the data read/write times for this type of device were slow when compared to optical discs. Later work used a metallized cantilever, with a radius of curvature of approximately 100 nm, in an AFM to perform charge reading/writing experiments [44]. From this and previous work [45] it was shown that the threshold voltage for erasing charge was strongly dependent on the thickness of the oxide layer, but the threshold voltage for charge writing was not. An array of 202 bits was used to spell out the words 'charge storage' in an area  $7\ \mu\text{m} \times 3\ \mu\text{m}$ . This work was later extended to cover an area of  $120\ \mu\text{m} \times 120\ \mu\text{m}$  with 24 189 bits, and also an area of  $90\ \mu\text{m} \times 90\ \mu\text{m}$  by 49 194 bits of information, using  $-40\ \text{V}$  pulses of 20  $\mu\text{s}$  duration [24]. The average distance between charged points was then just over 40 nm, and so the individual charge packets rather less than 40 nm. Tracks were also etched into the nitride layer to assist with tip positioning. Work by other authors produced similar bit arrays [16].

In studies on the long-term lifetime of the stored charges [46]  $-40\ \text{V}$  pulses ranging in duration from 90 to 1  $\mu\text{s}$  were applied to a 4.4 nm oxide layer NOS, and trapped charge was still present after storage at 150 °C for 9 months. It was not possible to determine the amount of charge decay, only that some trapped charge remained and that no appreciable charge spreading was seen. Separate experiments showed a decrease of 25% in the stored charge under the same conditions. The diameters of the trapped charge sites decreased with the pulse width, such that a 1  $\mu\text{s}$  pulse gave a spot size of 150 nm diameter. The shortest pulse widths used for writing were 40 ns, the limit of the pulse generator, but no results using this

value were presented. Similar work [47] used conducting cantilevers cut from 5  $\mu\text{m}$  tungsten foil which were then electrochemically etched to a point. Arrays of charge bits were written into NOS structures with oxide layers 5.1 nm and 6.6 nm thick, using pulses between  $-35$  and  $-38\ \text{V}$  and 100 and 20  $\mu\text{s}$  duration. This study concluded that the apparent spot size depended on three parameters; (a) the size of the metal tip/electrode, (b) the applied pulse height and width and (c) the bias applied during imaging.

### 3.4. ONOS (oxide-nitride-oxide-silicon) structures

A recent development in layered silicon based electrets shows promise for our purpose. It has been deduced that the stored charges in silicon based electrets are trapped in the interface between the nitride and oxide layers. Therefore in an oxide-nitride-oxide-silicon (ONOS) structure, shown schematically in figure 3(b), the charges would be trapped closer to the surface than for the older NOS structures, at the upper nitride-oxide interface. The interest in charge writing applications appeared to have declined, but the ONOS structure may herald a revival. The total thickness of the layers is usually between 16–20 nm, with the oxide layers typically 2–5 nm thick and the nitride layer 10 nm thick [48, 49].

Charge storage in ONOS was investigated as early as 1994 [44] in a general study of contact electrification of silicon-based layered media, work concentrating on the dissipation of electrons deposited on the surface. The data storage application was not looked into until 1996 [49], with the specific intention of using the AFM cantilever in non-contact mode when reading back the stored bits, to avoid the tip wear associated with earlier attempts in NOS structures. Using voltages of up to  $\pm 10\ \text{V}$  and pulse duration of 2–10 ms, bit sizes down to 100 nm in diameter (80 nm FWHM) could be written consistently, using both positive and negative bias. As this work concerned high density data storage, particular attention was paid to the data retrieval times, probably at the expense of resolution.

### 3.5. Other media

Most research into suitable materials for charge-induced data storage applications other than layered silicon structures or polymer electrets is irrelevant here as it does not actually involve charge storage, relying on, for example, a local change in chemical properties [19] or a phase change resulting in different electrical conductivity [23]. Charge dots with a 70 nm FWHM have been written to a 100 nm thick  $\text{SrTiO}_3$  film on a single crystal MgO substrate using contact electrification, but the charges decayed within 17 min [50]. Another worthwhile investigation [51] looked at surface modifications of  $\text{WSe}_2$  semiconductors using an STM, which preserved lateral atomic order, but produced mounds or ring-shaped features depending on the pulsed voltage. The authors ruled out material transfer and it is possible that the observed structures were due to stored charge. If so, this is quite promising as the features were small in size, from 1 to 8 nm diameter, and showed no evidence of decay even after 2 days. However, it remains to be confirmed that they were electrical charges rather than physical structures.

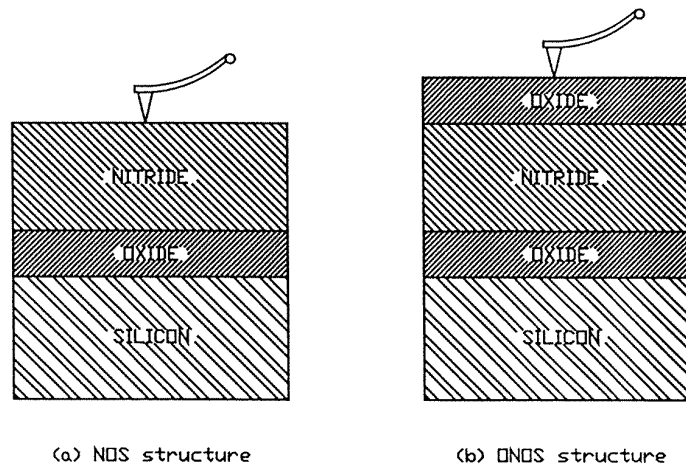


Figure 3. Layered structure electrets on silicon (a) NOS, (b) ONOS.

#### 4. Discussion

Returning now to the question posed by the title, it appears that only an SPM writing charge onto an electret is likely to offer serious prospects of microlocation or manipulation in the near future. Furthermore, the use of STM as envisaged by the early workers is not practical: it is difficult to control tip height in the presence of an insulator, the extra gap increases the pulse amplitude and duration needed, and the tunnelling current may adversely affect charge localization. There is significant likelihood of the physical surfaces being modified. By using a metallized AFM cantilever in contact when charge writing, the pulse amplitude and duration are kept to a minimum and there is little chance of surface damage. When scanning with an AFM it is also possible to measure simultaneously the charge profile and the topometric data, so that it is immediately apparent whether any physical surface modifications have occurred during charge writing.

The potential use of AFM-electret systems for manipulation is virtually absent from the literature. In 1992 Bergasa and Sáenz [52] speculated about generating anchoring points for proteins on surfaces using charge writing in an NOS system and concluded that it was not practical. Significantly, they acknowledged Quate for 'stimulating discussions on the charge storage problem' so it seems that at least some of the foremost researchers in the field also felt the idea too speculative to pursue. At that time they were almost certainly correct. The resolution of the charge writing techniques available was too large for the application proposed, although applications to submicrometre particles larger than protein molecules may have been underestimated. Also the stored charges were buried too deep in the NOS structure to readily attract particles to the substrate. However, recent studies of ONOS structures for charge storage [48, 49] claim that the charges are stored much closer to the surface of the substrate and could be imaged using a non-contact technique, suggesting that a useful intensity of electric field from each charge region now protrudes much further from the surface than before. To our knowledge, there has been no quantitative

study into the distribution of charge extending away from the surface of the substrate into the surrounding medium. One study [44] included an electrostatic simulation in a NOS structure with a 1–2 nm thick oxide layer and a 50 nm thick nitride layer that showed the charge was confined to an area of 50 nm diameter although the electrostatic potential extended to nearly 200 nm diameter within the NOS layers. The extent of the stored charge normal to the surface could be easily verified experimentally, by measuring the deflection of a biased cantilever (EFM) at different heights above the substrate for charged areas written with different bias voltages and pulse durations but seems not yet to have been done.

The multilayered electrets are currently the best choice for substrates, as the charged areas are relatively small (60–150 nm) and the charges persist for days or months. Although the smallest spot sizes were obtained in the NOS structures, the ONOS electret is relatively new and has not been researched as thoroughly. All the work on them has been for high density data storage applications, where data transfer rates are critical. It may well be possible to reduce the size of the charged areas if read and write times are relatively unimportant. It may also be possible to vary the charge concentration, so that similarly sized areas of charge have different electrostatic forces associated with them. Generally, no one material has a dominant likelihood of allowing smaller spot sizes, although as shown in figure 4 there is a general tendency for sizes to reduce as research progresses. Most polymer layers seem unsuitable because they have larger charge areas, but thin spun PMMA [29] and acetylene [32] have yielded small structures, as have organic dot molecules [34], although the smaller charged dots were not easy to produce.

The parameters used for charge writing vary considerably, even when using similar substrates, see tables 1–5. For polymer electrets, the variation in applied voltage and pulse duration is high: 0–300 V and 500  $\mu$ s to 20 s. Other materials are associated with lower voltages, typically 4–5 V for the single layer oxide electrets, 40–50 V for the NOS structures and <10 V for the ONOS layers. This may reflect a deliberate attempt to achieve readable/erasable

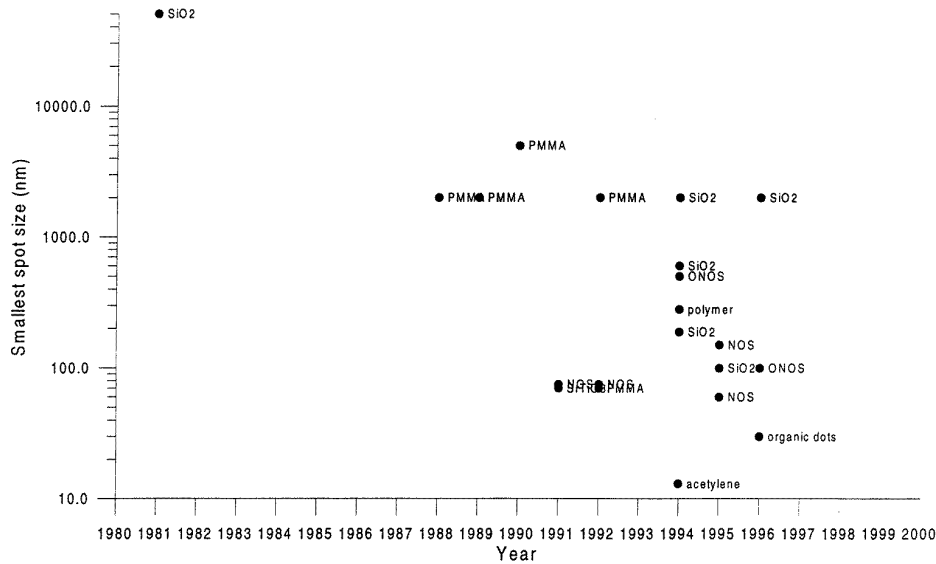


Figure 4. Stored charge spot-sizes for different electrets and years of reporting.

charge storage using voltages typically available in modern microelectronics. There is likely to be a threshold voltage for writing for each electret material. Using higher voltages will result in large charged areas, as the charge density at the tip will exceed this threshold over a larger area. It also appears that pulses with shorter duration produce smaller areas of stored charge, although no comprehensive study of this has been attempted. Longer pulses may allow the charge to diffuse through the substrate and produce larger charged areas. There seems need of a compromise between pulse duration and voltage, probably due to the actual amount of charge required for writing.

It remains a speculation whether a successful programmable nanomanipulation system can be based upon charge writing, but recent developments in materials technology should at the very least cause a re-evaluation of the pessimistic conclusions drawn a few years ago. There is now enough promise that experimental investigations are well justified. An AFM with a metallized cantilever should be used for the charge writing. Prefabricated tips coated first with Cr and then Au seem appropriate: they are relatively sharp, with typical (coated) tip radii of 25 nm or less. The recommended substrate, at least initially, is a multilayered ONOS structure. This electret produced some of the smallest (100 nm) charged areas with an indefinite storage lifetime, and could be scanned using a non-contact technique as the charges were trapped so close to the surface. The best pulse voltage and duration is not clear, but 100 nm diameter (80 nm FWHM) spots can be produced using 10 V, 2 ms pulses [49] and this is a sound base from which to start. It is highly likely that optimization of the charge writing parameters could produce spot sizes below 50 nm, and perhaps much smaller. With this level of resolution it would be relatively simple to write charge patterns to selectively trap particles with dimensions of a few hundred nanometres.

### Particle Grading

#### Digital or Analog Patterning

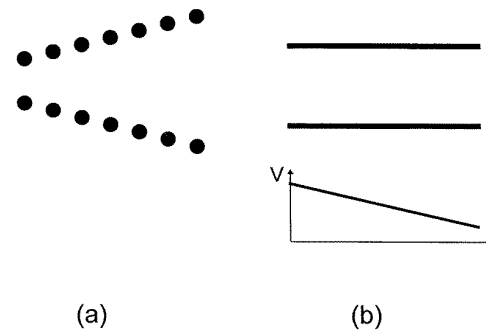


Figure 5. A tapered pattern for particle grading by digital and analogue methods.

### 5. Concluding remarks

While contact-mode writing to an ONOS structure, building directly on the experience of memory systems is our primary recommendation for immediate consideration, other technologies should not be ignored. For example, all current work has been on digital realizations, whereas if charge is stored with sufficient lateral stability analogue writing might be exploited. Lines and circles could then be written in vector form rather than as dot-matrices as shown in figure 1. Consider the elementary illustration in figure 5. We might wish to grade particles according to size by using a pair of non-parallel charge lines to trap them. One way is to have uniform (sampled or continuous) lines set at suitable angles, another is to maintain parallel physical



lines which have a steadily increasing charge density along them. The latter might be more effective if it results in more intense fields further from the surface. Other materials may be more suitable than ONOS structures in the longer term and for smaller features, perhaps polymer electrets such as plasma-polymerized acetylene [32]. The charge confining properties of the organic dots [34] might be adaptable to silicon based electrets—ONOS layers could be micromachined to leave tiny pillars of the correct dimensions in the desired locations that could be written with an SPM without the charge spreading to surrounding areas. Perhaps a thin spun layer of a piezoelectric polymer such as polyvinylidene difluoride (PVDF) could be selectively poled using a SPM tip to produce a permanent charge in the electret. It is not immediately apparent how this localized poling might be achieved but it is, for example, technically feasible to incorporate a thin film heater into the substrate to take the film over its Curie point.

There now seems to be a compelling case for thorough investigation of nanometric location and manipulation of small particles by these methods, which had been deemed impractical with the previous generation of charge-writing techniques. It would be surprising indeed if no significant scientific and technical developments arose from such investigations.

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